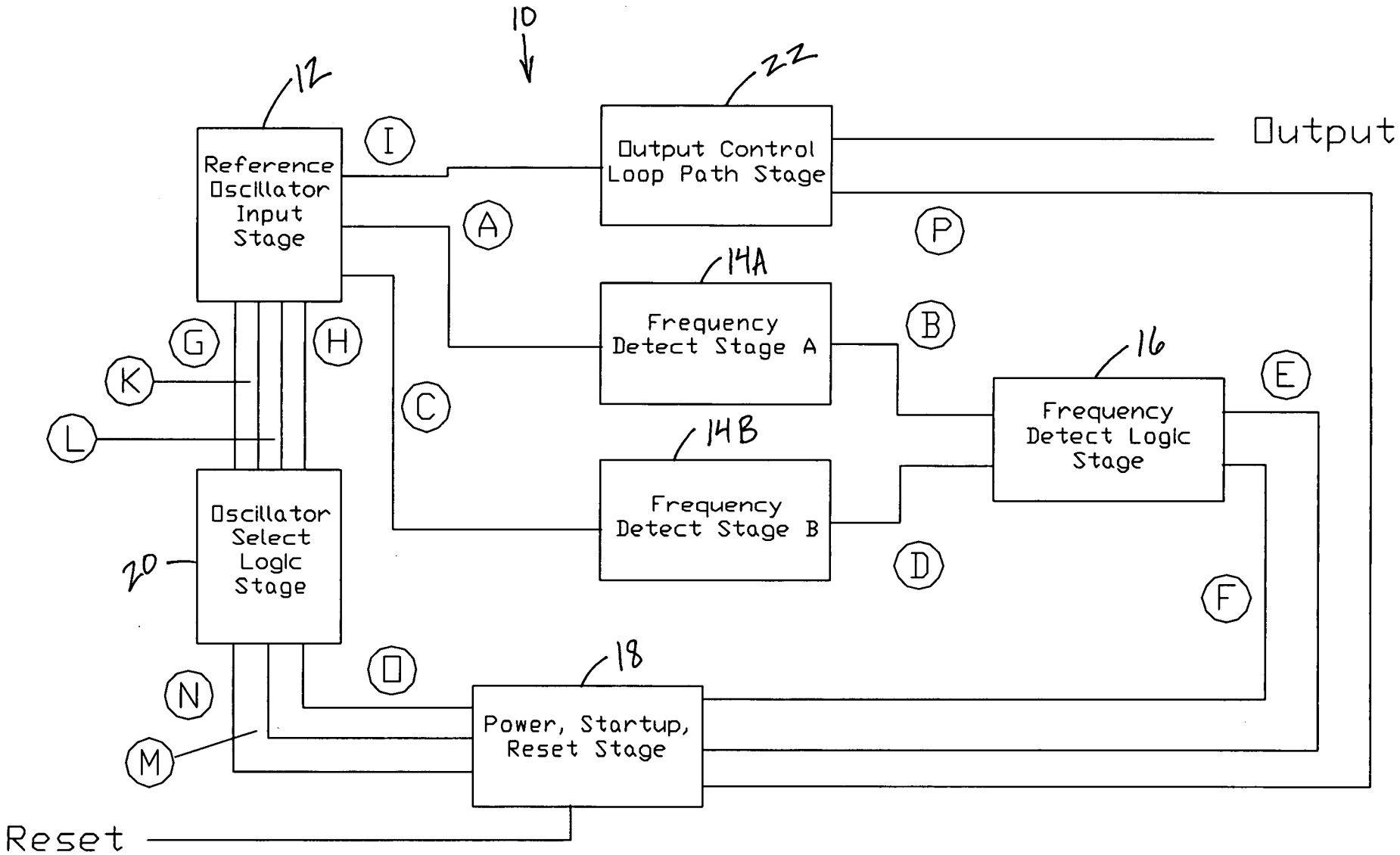

Figure 1 - Redundant Clock Module Block Diagram

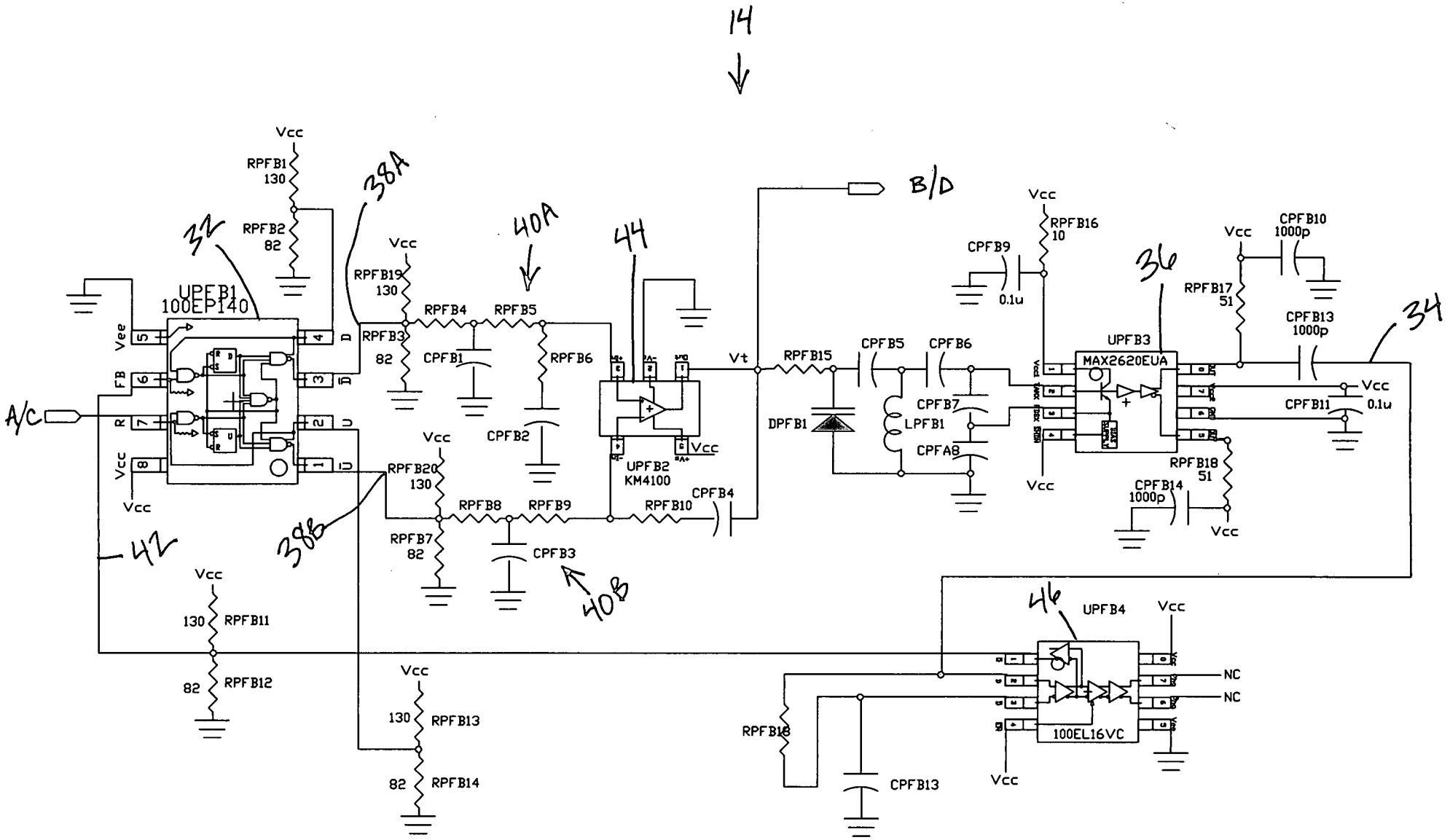

Figure 2 Frequency Detect Stage (A or B)

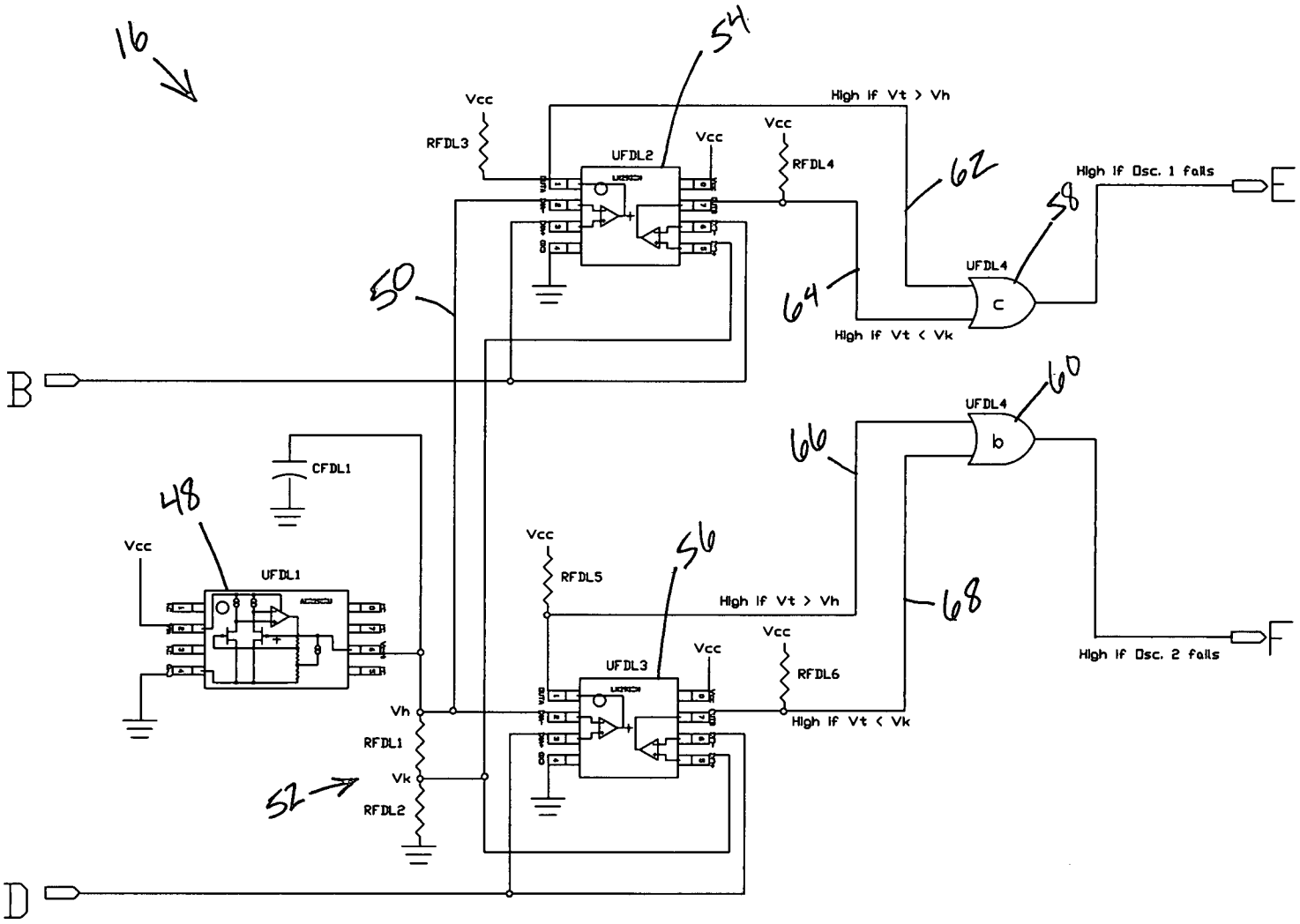

Figure 3 Frequency Detect Logic Stage

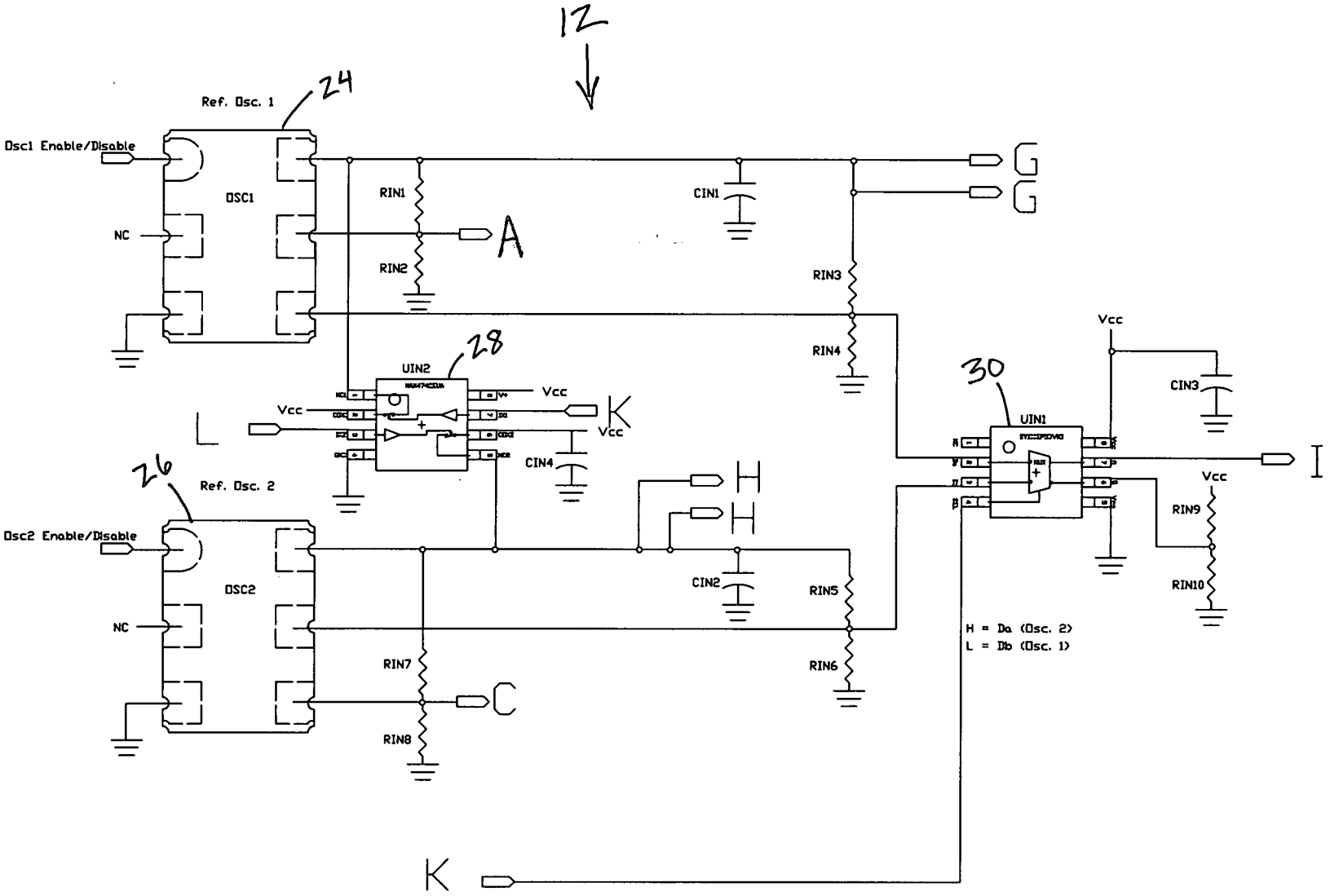

Figure 4 Reference Oscillator Input Stage

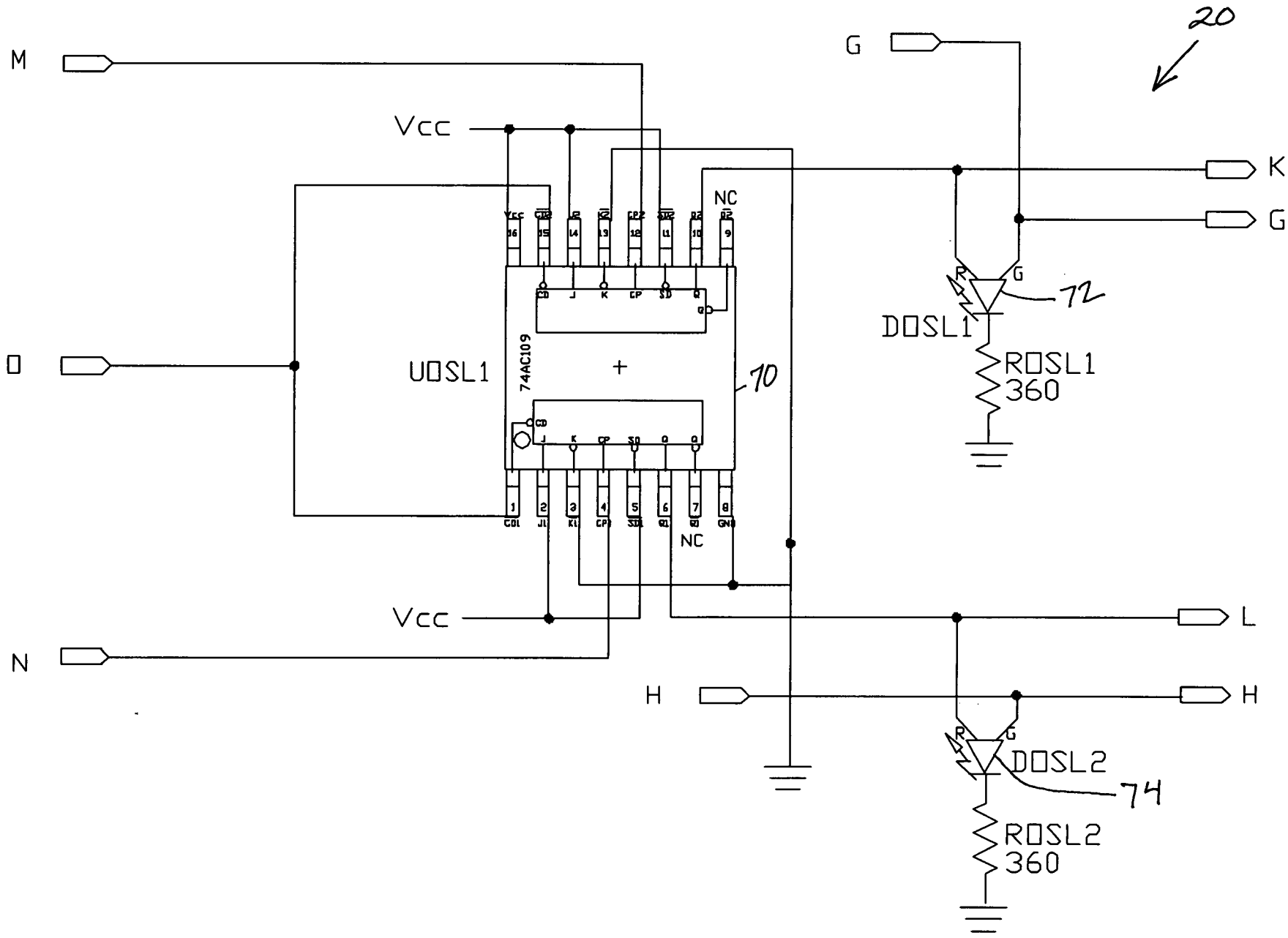

Figure 5 Oscillator Select Logic Stage

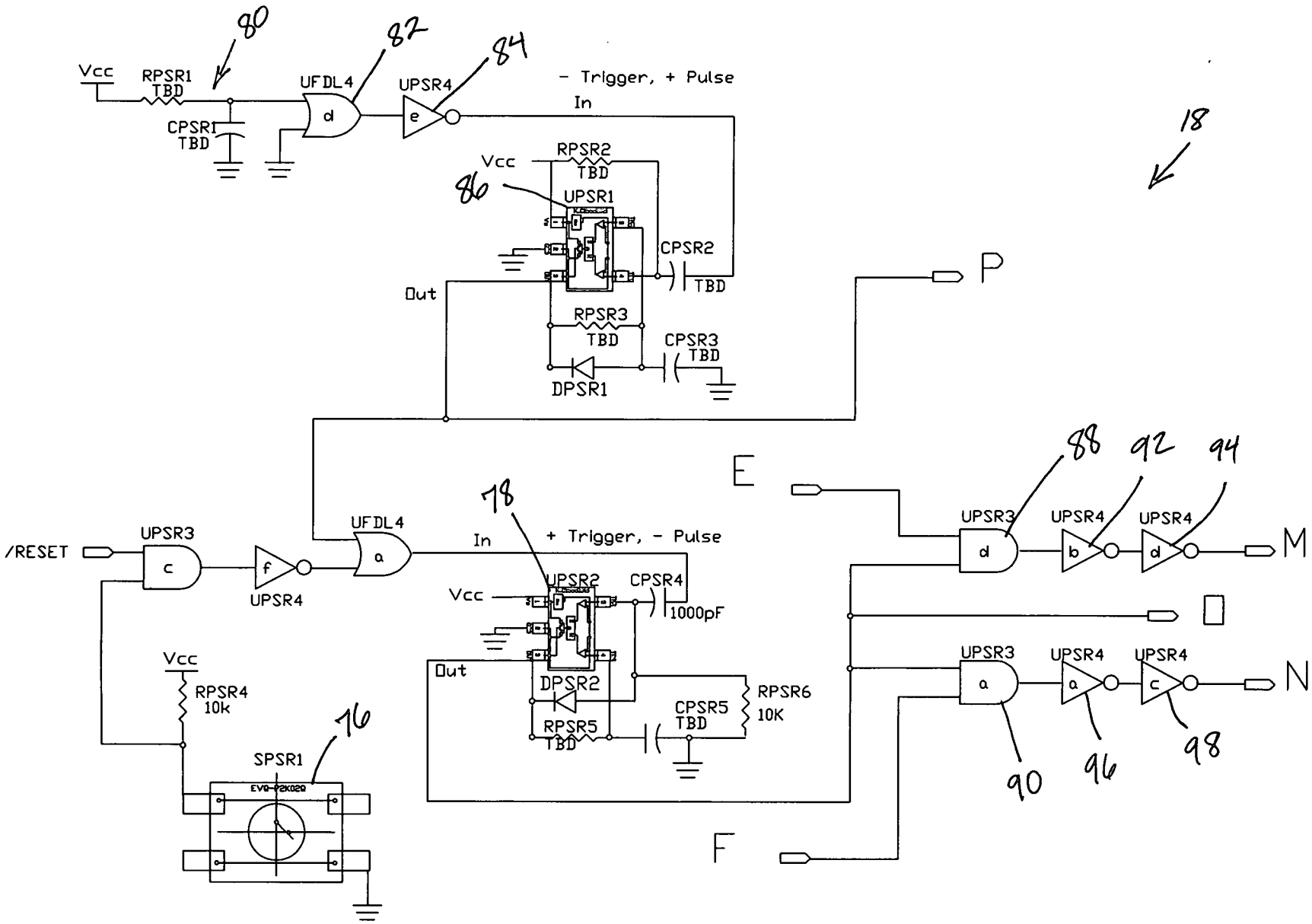

Figure 6 Power, Startup, Reset Stage

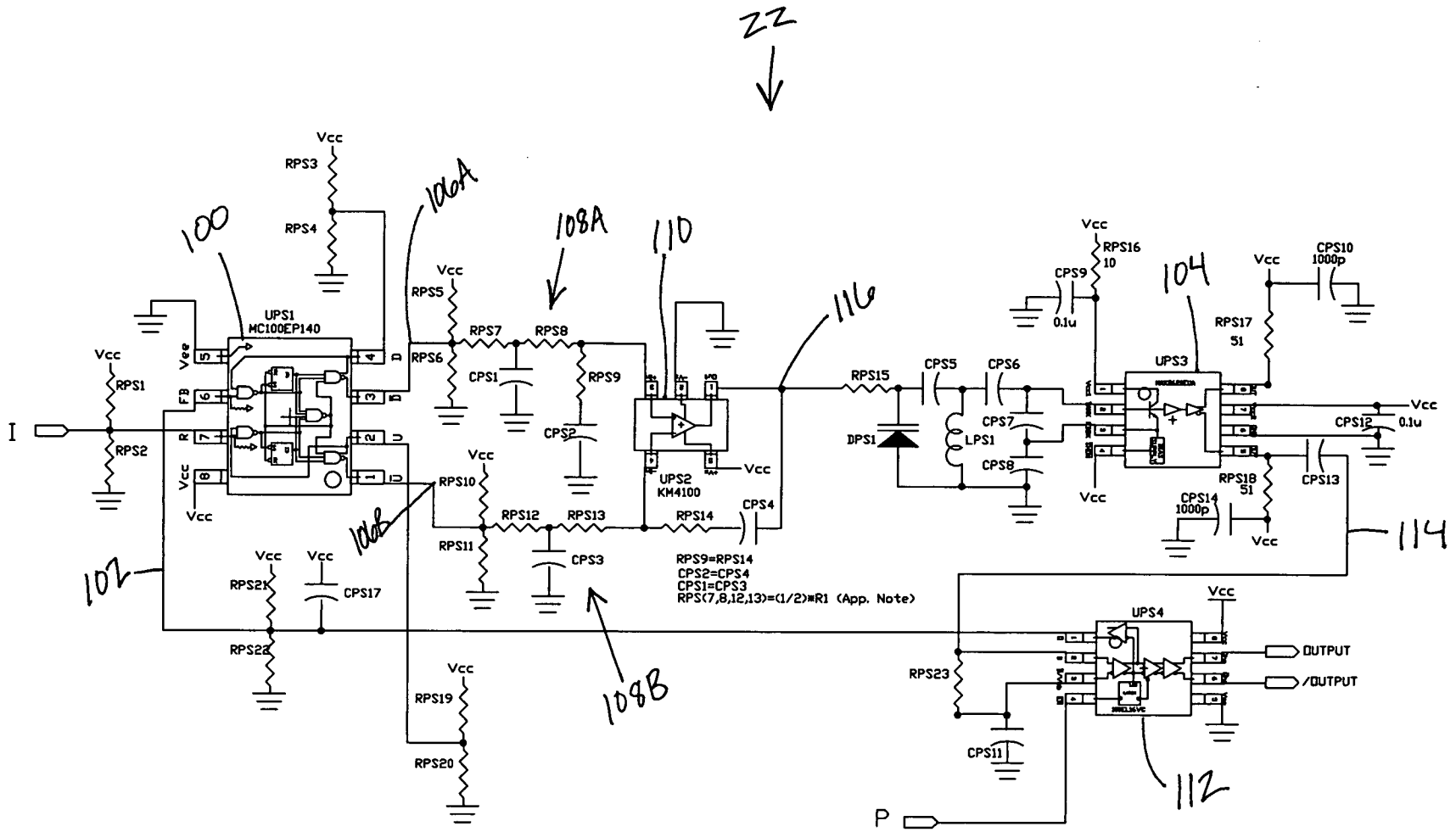

Figure 7 Output Control Loop Path Stage